IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Applicant(s): Balvinder Singh, et al.

Serial No.: 10/649,315

Filed: August 27, 2003

For: Combined Inverse Fast Fourier Transform And Guard Interval Processing For Efficient Implementation of OFDM Based Systems

Group No.: 2616

Confirmation No.: 5402

Examiner: Christopher P. Grey

Attorney
Docket No.: 7416/89890

AMENDED BRIEF ON APPEAL

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Real Party In Interest

Sasken Communication Technologies Limited is the assignee of the present application and is the real party in interest.

Related Appeals and Interferences

There are no related appeals involving the present application. Applicant is not aware of any interferences involving the present applications.

Status of Claims

Claims 1, 3-17, 19-22, and 24-33 are pending. Claims 2, 18, and 23 have been canceled. Claims 1, 3-6, 10-17, 19-22, and 24-33 stand rejected. The rejection has been made final. Claims 7-9 stand objected to as depending from rejected claims. A request for reconsideration was filed after the final rejection. No response to the request for reconsideration has been received. Accordingly, it is believed that the claims are currently under final rejection.

Status of Amendments

No amendments were made after the final rejection. A list of claims as presently amended is attached as an Appendix hereto.

Summary of Claimed Subject Matter

In certain implementations of circuits that convert frequency domain information to time domain information, it is desirable to shift data samples by a number of samples to insert a guard interval. In previously known circuits, a multiplier is appended to the input side of the IFFT circuit to multiply inputs to the Inverse Fast Fourier Transform circuit by a coefficient $e^{jK_i\tau}$ to achieve a circular shift. The claimed invention improves upon the prior art techniques for inserting a guard interval by reciting, among other things, an Inverse Fast Fourier Transform circuit that itself is adapted to circularly shift the input data by a number of samples. As explained in the present invention, modifying the IFFT circuit to perform a circular shift is advantageous as compared to appending a multiplier to multiply inputs by rotator coefficients because a modified IFFT avoids the complexity of an extra multiplier and, if done as described according to the present invention, would not add to the complexity of the IFFT circuit. See, Application, Paragraph 0052 ("the IFFT 208 may be modified (without increasing complexity), and the Rotator Coefficient 206, and Multiplier 202 may be eliminated in order to obtain a circularly shifted output").

With respect to the claimed subject matter, claim 1 claims a circuit for converting frequency domain information to time domain information including an Inverse Fast Fourier Transform circuit having a length of N samples. One example of an Inverse Fast Fourier Transform circuit is identified by reference numeral 208 in Fig. 12. A more detailed example of an IFFT Pipeline is illustrated in Fig. 13, identified by reference numeral 220. The Inverse Fast Fourier Transform circuit of claim 1 is

adapted to receive input data of length N samples, to circularly shift the input data by m samples, and to generate output data of length N samples that are circularly shifted by m samples. This is found in the Application at paragraph 0049.

Examples of a Cyclical Prefix Insertion circuit which is adapted to insert a cyclical prefix of length m are described in the Application at paragraphs 0050-54, for example. The Cyclical Prefix Insertion circuit has a first switch (210), connected to the Inverse Fast Fourier Transform circuit (208); buffer (212), has an input connected to the first switch and an output. The buffer has a length m. The Cyclical prefix Insertion circuit further includes a second switch (214), which is coupled to the first switch and to the buffer. The first and second switches selectively couple the output of the buffer and the Inverse Fast Fourier Transform circuit to an output of the second switch. These elements are illustrated in the drawing, for example, in Figs. 12 and 14.

In conventional IFFT pipelines, the butterfly units output the result of the addition first, and output of the subtraction second. The present application, in contrast with known IFFTs, discloses that changing the order of these operations, under certain circumstances, can cause a circular shift. This change is accomplished by appropriate change in the control circuitry and memory contents of the multiplier circuit with memory for the IFFT butterfly pipeline. For example, it is explained in paragraphs 0059-0065 that for certain cases, the circular shift may be obtained by modifying twiddle factor coefficients and the control for the rotator circuits. See also, Figs 16-20. In another example, it is explained in paragraphs 0066-0072 that controls may be modified to change the order of the operations so that the output of the subtraction operation of the butterfly circuit is output first, and the output of the addition operation is output second. Either of these modifications, along with modifications to the controls for the rotator circuits, can implement a desired circular shift without a separate multiplication step added before the IFFT circuitry to modify input samples with rotator

coefficients. Modifying the IFFT circuits using either of these examples may achieve the desired circular shift without the disadvantages of appending a multiplier of the input of the IFFT circuit.

Further examples which allow implementation of circular shifting by modifying the IFFT pipeline are found in claims 10 and 11. As explained in paragraph 0065 and Fig. 21, circular shifting may be obtained when the length of N samples of the Inverse Fast Fourier Transform and the cyclical prefix has a length m equal to N/4, and a control for a first rotator circuit is modified to effect the shift of the samples at the output of the Inverse Fast Fourier Transform by m samples. Paragraph 0072 describes an additional example where the N samples of the Inverse Fast Fourier Transform is equal to 64 and the cyclical prefix has a length m equal to 16.

Claim 13 claims a circuit for converting frequency domain information to time domain information including an Inverse Fast Fourier Transform circuit having a length of N samples. An Inverse Fast Fourier Transform circuit is identified by reference numeral 208 in Fig. 12. An example of an Inverse Fast Fourier Transform circuit configured as claimed in claim 13 is illustrated in Fig. 13, reference numeral 220. The Inverse Fast Fourier Transform circuit of claim 13 is adapted to receive input data of length N samples, where N is a power of 2 and the N samples are not multiplied by rotator coefficients, and implementing an algorithm selected from the group consisting of Radix-2 and Radix-2^2 algorithms. This is found in the Application at paragraph 0052. Examples of shifting the output of the transform circuit by m samples by modifying the control to a first stage rotator circuit and modifying the memory contents of the multiplier circuit, where m is less than N, are described in the Application at paragraphs 0052-57, for example. As illustrated in Fig. 12, the IFFT circuit 208 has an input that receives frequency domain information from Multiplier 202. In the example in Fig. 13, the Multiplier 202 is eliminated, and data path 222 indicates that the input to the IFFT 220 is made directly to leftmost Butterfly Circuit 224. The output is made at rightmost Butterfly Circuit 224.

An example of a guard interval insertion circuit may be found in the Application at paragraphs 0050-54, and in particular, in paragraph 0051. Therein, a switch 210 selectively switches an output of an IFFT to Buffer 212 and to switch 214. As illustrated in Fig. 14, the switches and the buffer allow reproducing and re-ordering the sequence of selected samples to insert a guard interval.

Claim 17 claims a circuit for converting frequency domain information to time domain information including a means for performing a circularly shifted Inverse Fast Fourier Transform on frequency domain information to generate time domain information, wherein the circular shift is approximately the same as a desired cyclical prefix and input samples for the Inverse Fast Fourier Transform are not multiplied by rotator coefficients. The one example of a means corresponding to this function is provided in Fig. 13, reference numeral 220, and described in the written description at 0052-53. Structure for this means is further described in paragraphs 0059-72. In one example, it is explained in paragraphs 0059-0065 that for certain cases, the circular shift may be obtained by modifying twiddle factor coefficients and the control for the rotator circuits. See also, Figs 16-20. In another example, it is explained in paragraphs 0066-0072 that controls may be modified to change the order of the operations so that the output of the subtraction operation of the butterfly circuit is output first, and the output of the addition operation is output second. Either of these modified IFFT circuits, along with modifications to the controls for the rotator circuits, can provide the means to implement a desired circular shift without a separate multiplication step added before the IFFT circuitry to modify input samples with rotator coefficients.

The first switch and second switch of claim 17 may be found as switch 210 and switch 214, respectively. See paragraph 0051 and Figs. 12, 14. Structure corresponding to the means for buffering may be found as Buffer 212. See paragraph 0051, Figs. 12, 14.

The present application, in claims 19 and 20, discloses that changing the order of the operations of the butterfly circuits, under certain circumstances, can cause a circular shift. This change is accomplished by appropriate change in the control circuitry and memory contents of the multiplier circuit with memory for the IFFT butterfly pipeline. For example, it is explained in paragraphs 0059-0065 that for certain cases, the circular shift may be obtained by a plurality of butterfly circuits, rotator circuits and multiplier circuits with memories, all coupled to a control circuit and a means for modifying a control for the first rotator circuit and memory contents of the first multiplier circuit with memory. See also, Figs 16-20. In another example, it is explained in paragraphs 0066-0072 that controls may be modified to change the order of the operations so that the output of the subtraction operation of the butterfly circuit is output first, and the output of the addition operation is output second.

Claim 22 is a method claim. The step of performing a circularly rotated Inverse Fast Fourier Transform on frequency domain information to generate time domain information without multiplying input samples by rotator coefficients may be found at paragraphs 0052. An example of the step of storing time domain information for a number of clock cycles may be found at paragraph 0057. Examples of steps of outputting time domain information as required by the last two steps of claim 22 may also be found in paragraph 0057. See also, Fig. 14.

Claims 26 and 30 are directed to a circuit adapted to, among other things, receive input data of length N samples, where N is a power of 2 and the N samples are not multiplied by rotator coefficients, and implementing an algorithm selected from the group consisting of Radix-2 and Radix-2^2 algorithms. The circuits of claims 26 and 30 are disclosed in the same portions of the specification associated with claims 1 and 13. See, e.g. paragraphs 0052 – 0057; Fig. 12, reference numeral 208; and Fig. 13, reference numeral 220.

Grounds Of Rejection To Be Reviewed On Appeal

The rejection of Claims 1 and 21-22 under 35 U.S.C. §103(a) as being unpatentable over Mazzoni et al., U.S. Pub. No. 2004/0151110.

The rejection of Claims 3, 10 and 11 under 35 U.S.C. §103(a) as being unpatentable over Mazzoni in view of admitted prior art and further in view of Walton et al., U.S. Pub. No. 2004/0081131.

The rejection of Claims 4, 5, and 6 under 35 U.S.C. §103(a) as being unpatentable over Mazzoni in view of admitted prior art, further in view of Walton, and further in view of Yeh, U.S. Pub. No. 2004/0059766.

The rejection of Claim 17 as being unpatentable over Yeh in view of prior art disclosed in the present application.

The rejection of Claims 19, 20, 24 and 25 under 35 U.S.C. §103(a) as being unpatentable over Mazzoni in view of admitted prior art and further in view of Yeh.

The rejection of Claims 26-33 under 35 U.S.C. §103(a) as being unpatentable over Yeh in view of Mazzoni.

The rejection of Claims 13-16 under 35 U.S.C. §103(a) as being unpatentable over Yeh in view of Mazzoni and further in view of the prior art disclosed in the present application.

The rejection of Claims 17, 19-22, and 25 under 35 U.S.C. §112, first paragraph as failing to comply with the written description requirement.

Argument

Claims 1 and 21-22 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Mazzoni et al., U.S. Pub. No. 2004/0151110, in view of admitted prior art. Claim 1 is patentable because claim 1 recites that the Inverse Fast Fourier Transform circuit itself is adapted to circularly shift the input data by m samples. The cited prior art, either alone or in combination, fails to disclose all of the elements of claim 1, e.g., an IFFT that itself is adapted to circularly shift input data by m samples, rather than relying on a circular shift performed prior to input to the IFFT.

For example, Mazzoni discloses a Fast Fourier Transform circuit which is not configured to circularly shift anything. Instead, in Mazzoni, a separate multiplier (reference numeral 22) is appended to the input of the FFT circuit to **multiply the input samples with rotator coefficients *before* the data samples are input to the fast Fourier transform circuit**. In this regard, Mazzoni discloses nothing more than a conventional FFT circuit. In contrast, in the present invention, the IFFT pipeline is modified in such a way to provide a new IFFT pipeline that achieves a circular shift by altering the memory contents and controls for the various structures inside the IFFT pipeline so that a circular shift can be achieved without an external rotator coefficient multiplier.

For example, in one embodiment of the invention, the IFFT changes the order of the addition and subtraction operations of the butterfly circuits, under certain circumstances, to achieve a circular shift. In one embodiment, the change in the order of outputting the results of the operations is achieved through modifying the twiddle factor coefficients and the control for the rotator circuits. E.g., Application, ¶¶ 0059-0065. In another embodiment, the controls are modified to achieve the change in order. E.g., Application, ¶¶ 0066-0072. Such embodiments are specifically claimed in claims 4, 5, and 6, for example.

Neither Mazzoni, nor the other art cited with respect to the rejections of claim 1, disclose or suggest such modifications to an IFFT circuit. Instead, if anything, Mazzoni teaches away from the present invention by requiring the additions of a separate multiplier to rotate the data samples before they are input to the FFT circuit. Claim 1 should be allowed because the novel IFFT circuit, in combination with the other elements of claim 1, is not disclosed in the cited prior art.

Claim 21 stands rejected with Claim 1. Claim 21 depends from claim 17. Claim 17 is believed allowable for the reasons set forth below, which are incorporated herein by reference. Claim 21 is believed allowable because it depends from allowable base claim 17.

Claim 22 stands rejected with Claim 1. Claim 22 claims a method comprising, among other things, performing a circularly rotated Inverse Fast Fourier Transform on frequency domain information to generate time domain information ***without*** *multiplying input samples by rotator coefficients*. Mazzoni does not disclose the method claimed in claim 22 because Mazzoni performs a Fourier transform on a data samples that were previously rotated by **multiplying the data samples with rotator coefficients**. One aspect of the present invention involves modifying an IFFT pipeline so that the circular rotation is achieved within the IFFT pipeline, and not prior to the transform circuitry. Claim 22 is therefore allowable over Mazzoni and the prior art disclosed in the application.

Claims 3, 10 and 11 are currently under final rejection based on similar (erroneous) grounds for rejection of claim 1, coupled with an additional reference, Walton et al., U.S. Pub. No. 2004/0081131. Claim 3 depends from claim 1 and is believed allowable for the same reason as claim 1, that is, neither Mazzoni nor the prior art identified in the application teaches or discloses an Inverse Fast Fourier Transform circuit that is itself adapted to circularly shift the input data by m samples, and instead, Mazzoni relies on a circular shift performed **prior** to input to the Fourier transform circuitry. Walton does not fill the gaps in Mazzoni. In particular, Walton does not disclose an IFFT circuit that is arranged to perform a circular shift. Accordingly, claim 3 should be allowed.

Claim 10 should be allowed because it depends from allowable base claims 1 and claim 3. Claim 10 further claims a particular example of the present invention, where the length of N samples of the Inverse Fast Fourier Transform and the cyclical prefix has a length m equal to N/4, and a control for a first rotator circuit is modified to effect the shift of the samples at the output of the Inverse Fast Fourier Transform by m samples. Claim 11 depends from claim 10 and further claims a particular example of the present invention where the N samples of the Inverse Fast Fourier Transform is equal to 64 and the cyclical prefix has a length m equal to 16. These specific examples are not obvious, and are

examples which allow implementation of circular shifting by modifying the IFFT pipeline. These claims are believed allowable for these additional reasons.

Claims 4, 5, and 6 are currently under final rejection under 35 U.S.C. §103(a) as being unpatentable, in view of numerous references, including Mazzoni and Walton, and the art discussed in the background of the invention and further in view of Yeh, U.S. Pub. No. 2004/0059766. Claims 4, 5 and 6 depend from claim 1, and therefore include all of the limitations of claim 1 and should be allowed at least for the same reasons as independent claim 1. However, claims 4, 5, and 6 recite additional limitations not found in the cited art, and are patentable for these additional reasons.

For example, claim 4 recites that the Inverse Fast Fourier Transform is adapted to circularly shift the input data by m samples **by modifying the memory contents** for multiplier circuits with memory and **modifying the control for rotator circuits**. These circuits are part of the IFFT. Claim 5 recites the Inverse Fast Fourier Transform is adapted to circularly shift the input data by m samples by **modifying the control for the first rotator circuit** and **memory contents** of the first multiplier circuit with memory. These circuits are part of the IFFT. As set forth above, neither Mazzoni, Walton, nor the prior art disclosed in the present application teach or suggest modifying an IFFT in this manner to circularly shift the data by m samples. Yeh also fails to fill the gaps in Mazzoni, Walton and the prior art disclosed in the present application. In particular, Yeh does not teach or disclose a transform circuit that is adapted to circularly shift input data by m samples by modifying the control for the first rotator circuit and memory contents of the first multiplier circuit with memory. Accordingly, neither Mazzoni, Walton, nor the prior art disclosed in the present application, nor Yeh teaches or suggests the specific ways that the IFFT is modified as recited in claims 4 and 5, i.e., by modifying the memory contents for multiplier circuits with memory and modifying the control for rotator circuits (claim 4) or by modifying the control for the first rotator circuit and memory contents of the first multiplier circuit with

memory (claim 5). Claims 4 and 5 should be allowed for these reasons in addition to the reasons given with respect to claim 1.

Claim 6 recites another configuration of the IFFT to effect a circular shift of the output of the Inverse Fast Fourier Transform circuit by m samples. In particular, claim 6 recites a control circuit configured to modify the control to the rotator circuit and to selectively control the plurality of butterfly circuits whether the addition operation or the subtraction operation is output first in time. As set forth above, the cited passages of the cited references do not disclose such structure. In particular, with reference to the citation to Yeh, it is not relevant that Yeh discloses conventional butterfly circuits because Yeh does not disclose or suggest changing the order of the operation of conventional butterfly circuits to achieve a circular shift, as disclosed in the present application and claimed in claim 6. Claim 6 should be allowed for this reason, in addition to the reasons given with respect to claim 1.

Claim 17 stands rejected as being unpatentable over Yeh in view of prior art disclosed in the present application. Claim 17 recites a means for performing a circularly shifted Inverse Fast Fourier Transform on frequency domain information to generate time domain information, wherein the circular shift is approximately the same as a desired cyclical prefix and input samples for the Inverse Fast Fourier Transform are not multiplied by rotator coefficients. Yeh in view of disclosed prior art does not render claim 17 obvious because Yeh and the disclosed prior art, either alone or combined, do not teach or suggest a means for performing a circularly shifted Inverse Fast Fourier Transform on frequency domain information without multiplying input samples by rotator coefficients. Accordingly, claim 17 should be allowed.

Claims 19, 20, 24 and 25 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Mazzoni in view of admitted prior art and further in view of Yeh. Claims 19 and 20 depend from claim 17, and therefore include all of the limitations of claim 17 and are believed allowable for the

same reasons as independent claim 17. The remarks with respect to claim 17 as set forth above are incorporated herein by reference.

Claims 24 and 25 depend from claim 22, and therefore include all of the limitations of claim 22 and are believed allowable for the same reasons as independent claim 22. The remarks with respect to claim 22 as set forth above are incorporated herein by reference.

Claim 19 should also be allowed because claim 19 recites that the means for performing a circularly rotated Inverse Fast Fourier Transform further comprises a means for modifying a control for the first rotator circuit and memory contents of the first multiplier circuit with memory. As set forth above, neither Mazzoni, nor the prior art disclosed in the present application, nor Yeh teach or suggest a means for performing a circularly rotated Inverse Fast Fourier Transform that includes modifying an IFFT to circularly rotate the data. Accordingly, neither Mazzoni, nor the prior art disclosed in the present application, nor Yeh can teach or suggest the specific ways that the IFFT is modified as recited in claim 19, i.e., modifying a control for the first rotator circuit and memory contents of the first multiplier circuit with memory. Claim 24 should be allowed for similar reasons.

Claim 20 recites that the means for performing a circularly rotated Inverse Fast Fourier Transform further comprises a means for modifying the order of the contents of the memory and modifying the control circuit to modify the control of the rotator circuits and butterfly circuits. As set forth above, neither Mazzoni, nor the prior art disclosed in the present application, nor Yeh teach or suggest a means for performing a circularly rotated Inverse Fast Fourier Transform that includes modifying an IFFT to circularly rotate the data. Accordingly, neither Mazzoni, nor the prior art disclosed in the present application, nor Yeh can teach or suggest the specific ways that the IFFT is modified as recited in claim 19, i.e., by modifying the order of the contents of the memory and modifying the control circuit to modify the control of the rotator circuits and butterfly circuits. Claim

25 should be allowed for similar reasons.

Claims 26-33 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yeh in view of Mazzoni. Claim 26 claims, inter alia, that the output of the transform circuit is circularly shifted by m samples by modifying the control to a first stage rotator circuit and modifying the memory contents of the multiplier circuit. Claim 30 claims, inter alia, that the output of the transform circuit is circularly shifted by m samples by modifying the control to the butterfly circuit, modifying the control to the rotator circuit and re-ordering the memory contents of the multiplier circuit. As set forth above, Yeh and Mazzoni do not teach or suggest such structure. In particular, Mazzoni appears to rely on an external multiplier to multiply inputs to the IFFT by rotator coefficients before the data samples are entered into the transform circuit. Yeh, on the other hand, appears to re-order data using a "reordering circuit 1100," which is disclosed as a dual port RAM, to change the order of samples. Neither Mazzoni nor Yeh teach or disclose modifying a transform circuit to achieve a circular shift. Accordingly, claims 26 and 30, and the claims 27-29 and 31-33 that depend therefrom, should be allowed over those published applications.

Claims 13-16 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yeh in view of Mazzoni and further in view of the prior art disclosed in the present application. Claim 13, as presently amended, recites that the Inverse Fast Fourier Transform circuit has a length of N samples, where N is a power of 2 and the N samples are not multiplied by rotator coefficients. Claim 13 also recited that the Inverse Fast Fourier Transform circuit has a plurality of butterfly circuits, multiplier circuits with memory and rotator circuits, all coupled to a control circuit and is configured to circularly shift output information by m samples.

Claim 13 is patentable over Yeh and Mazzoni because neither Yeh, Mazzoni nor the prior art disclosed in the present application teach or suggest configuring an IFFT to circularly shift data by m

samples without multiplying the IFFT inputs by rotator coefficients. Furthermore, Yeh, Mazzoni nor the prior art disclosed in the present application teach or suggest configuring an IFFT having a plurality of butterfly circuits, multiplier circuits with memory and rotator circuits, all coupled to a control circuit and is configured to circularly shift output information by m samples. Accordingly, claim 13, and claims 14-16, which depend from claim 13 should be allowed.

Claims 17, 19-22, and 25 stand rejected under 35 U.S.C. §112, first paragraph as failing to comply with the written description requirement. This rejection is improper because the written description supports the claimed inventions.

The November 27, 2007 Office Action errs when it states, on page 2, that "the claimed limitation, 'and input samples for the IFFT are not multiplied by rotator coefficients' is not fully supported by the specification." The written description describes in detail at least two alternative ways to modify an IFFT to perform a circular shift without a discrete step of multiplying input data samples by rotator coefficients. Examples of such embodiments are claimed, for example, in claims 4, 5 and 6, discussed earlier in this paper.

In conventional IFFT pipelines, the butterfly units output the result of the addition first, and output of the subtraction second. The present application discloses that changing the order of these operations, under certain circumstances, can cause a circular shift. This change is accomplished by appropriate change in the control circuitry and memory contents of the multiplier circuit with memory for the IFFT butterfly pipeline. For example, it is explained in paragraphs 0059-0065 that for certain cases, the circular shift may be obtained by modifying twiddle factor coefficients and the control for the rotator circuits. In another example, it is explained in paragraphs 0066-0072 that controls may be modified to change the order of the operations so that the output of the subtraction operation of the butterfly circuit is output first, and the output of the addition operation is output second. Either of

these modifications, along with modifications to the controls for the rotator circuits, can implement a desired circular shift without a separate multiplication step added before the IFFT circuitry to modify input samples with rotator coefficients.

In the alternative embodiment in Fig 13, when elements 202 and 206 (Fig. 12) are eliminated, there is still a multiplier 226. However, because this multiplier is ***within*** the IFFT, the samples which are input to the IFFT arrive at the IFFT without having been multiplied by rotator coefficients. Additionally, twiddle factor multiplier 226 in Fig. 13 for the IFFT pipeline is not the same as a rotator coefficient multiplier 202 at the input of the IFFT pipeline (Fig. 12) because no rotator coefficients are provided to the multiplier 226. For the above reasons, claims 17, 19-22, and 25 are supported by the written description, and should not be rejected under 35 U.S.C. §112.

For the reasons set forth above, the claims as currently presented are believed allowable. Applicants request that the rejections be reversed.

Respectfully submitted,

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December 12, 2008

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Claims Appendix

1. (previously presented) A circuit for converting frequency domain information to time domain information comprising:

a. an Inverse Fast Fourier Transform circuit having a length of N samples, the Inverse Fast Fourier Transform circuit adapted to receive input data of length N samples, to circularly shift the input data by m samples; and to generate output data of length N samples that are circularly shifted by m samples; and

b. a Cyclical Prefix Insertion circuit adapted to insert a cyclical prefix of length m, the Cyclical Prefix Insertion circuit having;

1. a first switch, connected to the Inverse Fast Fourier Transform circuit;

2. a buffer, having an input connected to the first switch and an output, the buffer having a length m; and

3. a second switch, coupled to the first switch and to the buffer, wherein the first and second switches selectively couple the output of the buffer and the Inverse Fast Fourier Transform circuit to an output of the second switch.

2. (canceled).

3. (previously presented) The circuit for converting frequency domain information to time domain information of claim 1 wherein the length of N samples is a power of 2 and wherein the Inverse Fast Fourier Transform circuit implements an algorithm selected from the group consisting of Radix-2 and Radix-2^2 algorithms.

4. (previously presented) The circuit for converting frequency domain information to time domain information of claim 3 wherein the Inverse Fast Fourier Transform circuit further comprises a plurality of butterfly circuits, rotator circuits and multiplier circuits with memories, all coupled to a control circuit, and the Inverse Fast Fourier Transform is adapted to circularly shift the input data by m samples by modifying the memory contents for multiplier circuits with memory and modifying the control for rotator circuits.

5. (previously presented) The circuit for converting frequency domain information to time domain information of claim 3 wherein the Inverse Fast Fourier Transform circuit further comprises a plurality of butterfly circuits, multiplier circuits with memory and rotator circuits, all coupled to a control circuit, and the Inverse Fast Fourier Transform is adapted to circularly shift the input data by m samples by modifying the control for the first rotator circuit and memory contents of the first multiplier circuit with memory.

6. (previously presented) A circuit for converting frequency domain information to time domain information of claim 3 wherein the Inverse Fast Fourier Transform circuit further comprises:

a. a plurality of butterfly circuits, multiplier circuits with memory and rotator circuits and coupled to an input, wherein each butterfly circuit is configured to perform an addition operation and a subtraction operation;

b. a control circuit configured to modify the control to the rotator circuit and to selectively control the plurality of butterfly circuits whether the addition operation or the subtraction operation is output first in time to effect a circular shift of the output of the Inverse Fast Fourier Transform circuit by m samples; and

c. the contents of the memory of the multiplier circuit with memory are arranged in a suitably modified manner.

7. (previously presented) The circuit for converting frequency domain information to time domain information of claim 3 wherein the length of N samples is segmented into first, second, third, and fourth segments of N/4 samples, wherein the circular shift m is equal to N/4 and is effected by multiplying the input N samples by unity for the first segment of N/4 samples, -1 for the second segment of N/4 samples, -j for the third segment of N/4 samples, and j for the fourth segment of N/4 samples.

8. (previously presented) The circuit for converting frequency domain information to time domain information of claim 7 wherein the first, second, third, and fourth segments of N/4 samples comprise the length of N samples in consecutive order.

9. (previously presented) The circuit for converting frequency domain information to time domain information of claim 7 wherein the N samples of the Inverse Fast Fourier Transform is equal to 64 and the cyclical prefix has a length m equal to 16.

10. (previously presented) The circuit for converting frequency domain information to time domain information of claim 3 wherein the length of N samples of the Inverse Fast Fourier Transform and the cyclical prefix has a length m equal to N/4, and a control for a first rotator circuit is modified to effect the shift of the samples at the output of the Inverse Fast Fourier Transform by m samples.

11. (previously presented) The circuit for converting frequency domain information to time domain information of claim 10 wherein the N samples of the Inverse Fast Fourier Transform is equal to 64 and the cyclical prefix has a length m equal to 16.

12. (original) The circuit for converting frequency domain information to time domain information of claim 1 wherein the cyclical prefix comprises a guard interval for an orthogonal frequency division multiplexing system.

13. (previously presented) A circuit for converting frequency domain information to time domain information comprising;

a. an Inverse Fast Fourier Transform circuit having:

1. an input adapted to receive frequency domain information;
2. an output providing time domain information;
3. the Inverse Fast Fourier Transform circuit having a length of N samples,

where N is a power of 2 and the N samples are not multiplied by rotator coefficients, and implementing an algorithm selected from the group consisting of Radix-2 and Radix-2^2 algorithms, the Inverse Fast Fourier Transform circuit further having a plurality of butterfly circuits, multiplier circuits with memory and rotator circuits, all coupled to a control circuit and configured to circularly shift output information by m samples, where m is less than N; and

b. guard interval insertion circuit adapted to insert a cyclical prefix of length m, the guard interval insertion circuit having;

1. a first switch, connected to the output of the Inverse Fast Fourier Transform circuit;

2. a buffer, having an input connected to the first switch and an output, the buffer having a length m; and

3. a second switch, coupled to the first switch and to the buffer, wherein the first and second switches selectively couple the output of the buffer and the output of the Inverse Fast Fourier Transform circuit to an output of the second switch.

14. (previously presented) The circuit for converting frequency domain information to time domain information of claim 13 wherein the Inverse Fast Fourier Transform circuit is configured to circularly shift output information by m samples by modifying the control for the first rotator circuit and memory contents of the first multiplier circuit with memory.

15. (previously presented) The circuit for converting frequency domain information to time domain information of claim 13 wherein the Inverse Fast Fourier Transform circuit is configured to circularly shift output information by m samples by modifying the order of the contents of the memory and modifying the control circuit to modify the control of the rotator circuits and butterfly circuits.

16. (previously presented) The circuit for converting frequency domain information to time domain information of claim 13 wherein the length of N samples of the Inverse Fast Fourier Transform is equal to 64 and the cyclical prefix has a length m equal to 16, and the modification is applied to control for the first rotator circuit of the Inverse Fast Fourier Transform circuit to circularly shift the output data by 16 samples.

17. (previously presented) A circuit for converting frequency domain information to time domain information comprising:

a. a means for performing a circularly shifted Inverse Fast Fourier Transform on frequency domain information to generate time domain information, wherein the circular shift

is approximately the same as a desired cyclical prefix and input samples for the Inverse Fast Fourier Transform are not multiplied by rotator coefficients;

b. a first switch, connected to the means for performing a circularly rotated Inverse Fast Fourier Transform;

c. a means for buffering a portion of the time domain signals approximately the same as the desired cyclical prefix, the means for buffering having an input connected to the first switch; and

d. a second switch, coupled to the first switch and to the means for buffering, wherein the first and second switches selectively couple the output of the means for buffering and the means for performing a circularly rotated Inverse Fast Fourier Transform circuit to an output of the second switch.

18. (canceled)

19. (previously presented) The circuit for converting frequency domain information to time domain information of claim 17 wherein the means for performing a circularly rotated Inverse Fast Fourier Transform further comprises a plurality of butterfly circuits, rotator circuits and multiplier circuits with memories, all coupled to a control circuit and a means for modifying the control for the first rotator circuit and memory contents of the first multiplier circuit with memory.

20. (previously presented) The circuit for converting frequency domain information to time domain information of claim 17 wherein the means for performing a circularly rotated Inverse Fast Fourier Transform further comprises a plurality of butterfly circuits, rotator circuits and multiplier circuits with memories, all coupled to a control circuit and a means for modifying the order of the contents of the memory and modifying the control circuit to modify the control of the rotator circuits and butterfly circuits.

21. (original) The circuit for converting frequency domain information to time domain information of claim 17 wherein the cyclical prefix comprises a guard interval for an orthogonal frequency division multiplexing system.

22. (previously presented) A method of generating circularly shifted time domain signal from frequency domain information in an Inverse Fast Fourier Transform circuit and having a desired cyclical prefix comprising:

a. performing a circularly rotated Inverse Fast Fourier Transform on frequency domain information to generate time domain information without multiplying input samples by rotator coefficients, wherein the amount of the circular shift is the same as the length of the cyclical prefix;

b. storing the time domain information for a number of clock cycles equal to the cyclical prefix in a buffer while simultaneously outputting the time domain information;

c. outputting the time domain information for a number of clock cycles equal to a length of the Inverse Fast Fourier Transform minus the length of the cyclical prefix; and

d. outputting the time domain information stored in the buffer for a number of clock cycles equal to the length of the cyclical prefix.

23. (canceled).

24. (previously presented) The method of claim 22 wherein the Inverse Fast Fourier Transform comprises a plurality of butterfly circuits, rotator circuits and multiplier circuits with memories, all coupled to a control circuit and the step of performing a circularly shifted Inverse Fast Fourier Transform further comprises modifying the control for the first rotator circuit and memory contents of the first multiplier circuit with memory.

25. (previously presented) The method of claim 22 wherein the Inverse Fast Fourier Transform comprises a plurality of butterfly circuits, rotator circuits and multiplier circuits with memories, all coupled to a control circuit and the step of performing a circularly shifted Inverse Fast Fourier Transform further comprises modifying [[the]] an order of the contents of the memory and modifying the control of the rotator circuits and butterfly circuits.

26. (previously presented) A transform circuit having a length of N samples, where N is a power of 2, and implementing an algorithm selected from the group consisting of Radix-2 and Radix-2^2 algorithms, the transform circuit further having a plurality of butterfly circuits, multiplier circuits with memory and rotator circuits, all coupled to a control circuit, wherein an output of the transform circuit is circularly shifted by m samples by modifying the control to a first stage rotator circuit and modifying the memory contents of the multiplier circuit, where m is less than N.

27. (original) The circuit of claim 26 wherein the transform circuit comprises a Fast Fourier Transform circuit.

28. (original) The circuit of claim 26 wherein the transform circuit comprises an Inverse Fast Fourier Transform circuit.

29. (previously presented) The circuit of claim 26 wherein the transform circuit is configurable as an Inverse Fast Fourier Transform circuit and as a Fast Fourier Transform circuit, wherein each configuration maintains the same circular shift of m samples.

30. (previously presented) A transform circuit having a length of N samples, where N is a power of 2, and implementing an algorithm selected from the group consisting of Radix-2 and Radix-2^2 algorithms, the transform circuit further having a plurality of butterfly circuits, multiplier circuits with memory and rotator circuits, all coupled to a control circuit, wherein an output of the transform circuit is circularly shifted by m samples by modifying the control to the butterfly circuit, modifying the control to the rotator circuit and re-ordering the memory contents of the multiplier circuit, where m is less than N.

31. (original) The circuit of claim 30 wherein the transform circuit comprises a Fast Fourier Transform circuit.

32. (original) The circuit of claim 30 wherein the transform circuit comprises an Inverse Fast Fourier Transform circuit.

33. (previously presented) The circuit of claim 30 wherein the transform circuit is configurable as an Inverse Fast Fourier Transform circuit and as a Fast Fourier Transform circuit, wherein each configuration maintains the same circular shift of m samples.

Evidence Appendix

Not Applicable.

Related Proceedings Appendix

Not Applicable.